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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/530,553	07/21/2000	GERALD DEBOY	POO0578	6916

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Schiff Hardin & Waite
Patent Department
7100 Sears Tower
CHICAGO, IL 60606-6473

EXAMINER
BROCK II, PAUL E

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/530,553	DEBOY ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16 and 20-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16 and 20-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *23* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The corrected or substitute drawings were received on December 2, 2002. These drawings are approved.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claim 31 is rejected under 35 U.S.C. 102(e) as being anticipated by Shinohe et al. (USPAT 5969400, Shinohe).

With regard to claim 31, Shinohe discloses in figure 12 a semiconductor chip. Shinohe discloses in figure 12 a substrate having a major surface. Shinohe discloses in figure 12 a field of high voltage semiconductor components (42, 45, 54, etc.) defining a high voltage portion in the substrate. Shinohe discloses in figure 12 an edge structure at an edge of the high voltage portion, the edge structure separating the high voltage portion of the substrate from an edge of the major surface of the substrate. Shinohe discloses in figure 12 at least one inner-zone of a first conductivity type defining a ring structure around the field of high voltage semiconductor components at the major surface. Shinohe discloses in figure 12 at least one floating guard ring of a second conductivity type arranged in the at least on inner zone. Shinohe discloses in figure 12 at least one inter-ring zone of the first conductivity type arranged in the at least one inner zone, the at least one inter-ring zone being adjacent to the at least one floating guard ring. Shinohe discloses in figure 12 at least one of the inter-ring zone and the floating guard ring being of at least on of a conductivity and a geometry such that their free charge carriers are totally depleted when a blocking voltage is applied.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 16, 20 – 23, 25 – 20 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinohe in view of Hshieh et al. (USPAT 5930630, Hshieh).

With regard to claim 16, Shinohe discloses in figure 12 a high voltage semiconductor component. Shinohe discloses in figure 12 a semiconductor body having a high voltage region and having an edge region of the high voltage region, a high voltage resistant structure at the edge region having at least one inner zone (portion between 47 and D, not 52) of a first conductivity type adjacent to a first surface of said semiconductor body. Shinohe discloses in figure 12 a cell field (portion under 49) including high voltage components in the high voltage region. Shinohe is silent to teaching that high voltage individual components are connected in parallel. Hshieh teaches in figures 5f a cell field (portion under S) including individual high voltage components (125) in a high voltage region, the high voltage individual components being connected in parallel (S) and arranged in individual cells. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the individual high voltage components of Hshieh in the device of Shinohe in order to improve device ruggedness as stated by Hshieh in column 3, lines 58 – 64. Shinohe discloses in figure 12 at least one floating guard ring (52) of a second conductivity type arranged in said inner zone, said at least one floating guard ring surrounding the cell field. Shinohe discloses in figure 12 at least one inter-ring zone (between 52's) of said first conductivity type respectively arranged in said inner zone, said at least one inter-ring zone being arranged adjacent the at least one floating guard ring. Shinohe discloses in figure 12 the at least one floating guard ring and said at least one inter-ring zone have at least one of conductivities and geometries set such that their free charge carriers are totally depleted when a blocking voltage is applied.

With regard to claim 20, Shinohe discloses in figure 12 wherein said at least one floating guard ring has a U-shaped cross section.

With regard to claim 21, Shinohe discloses in figure 12 at least one space charge zone stopper (51) located at an outermost edge of said edge region of said semiconductor component.

With regard to claim 22, Shinohe discloses in figure 12 wherein said space charge zone stopper comprises a heavily doped region (47) of said first conductivity type, said heavily doped region being arranged in said inner zone.

With regard to claim 23, Shinohe discloses in figure 12 wherein said space charge zone stopper comprises a damage implanted region (47) being arranged in said inner zone.

With regard to claim 25, Shinohe does not disclose a magnetoresistor. Hshieh teaches in figure 5f at least one magnetoresistor (125) located at an inner edge of an edge region of said semiconductor component. It would have been further obvious to one of ordinary skill in the art at the time of the present invention to use the magnetoresistor of Shinohe in order to improve device performance as taught by Hshieh in the paragraph linking columns 1 and 2.

With regard to claim 26, Hshieh teaches in figure 5f wherein at least one of said magnetoresistors is simultaneously a gate electrode of said semiconductor component.

With regard to claim 27, Hshieh teaches in figure 5f wherein at least an outermost of the magnetoresistors is nearly completely enclosed by a cathode metallization (170) in a direction of the first surface of the semiconductor component.

With regard to claim 28, Hshieh teaches in figure 5f wherein said cathode metallization is a metallization of a source electrode of said semiconductor component.

With regard to claim 29, Shinohe discloses in figure 12 wherein said inter-ring zones in said edge region have a cross-section tapered to said first surface.

With regard to claim 30, Hshieh teaches in figure 5f wherein the individual high voltage components are vertical power transistors.

With regard to claim 32, Shinohe discloses in figure 12 a semiconductor chip. Shinohe discloses in figure 12 a substrate having a major surface. Shinohe discloses in figure 12 a plurality of high voltage semiconductor components in the substrate. Shinohe is silent to teaching that high voltage semiconductor components are high voltage vertical MOSFET components. Hshieh teaches in figures 5f a plurality of high voltage vertical MOSFET components in the substrate. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the high voltage vertical MOSFET components of Hshieh in the device of Shinohe in order to improve device ruggedness as stated by Hshieh in column 3, lines 58 – 64. Shinohe discloses in figure 12 an edge structure at an edge of the plurality of high voltage semiconductor components to separate the high voltage semiconductor components from a remainder of the substrate. Shinohe discloses in figure 12 at least one inner zone of a first conductivity type defining a ring structure around the plurality of high voltage semiconductor components at the major surface. Shinohe discloses in figure 12 at least one floating guard ring of a second conductivity type arranged in the at least on inner zone. Shinohe discloses in figure 12 an inter-ring zone of the first conductivity type arranged in the at least one inner zone, the inter-ring zone being allocated to the at least one floating guard ring. Shinohe discloses in figure 12 at least one of the inter-ring zone and the floating guard ring being of at least on of a

conductivity and a geometry such that their free charge carriers are totally depleted when a blocking voltage is applied.

6. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shinohe and Hshieh as applied to claims 16 and 21 above, and further in view of Hsu et al. (USPAT 5521105, Hsu).

With regard to claim 24, Shinohe discloses in figure 12 wherein said space charge zone stopper comprises an electrode (51) connected to said inner zone. Hsu is silent to an electrode material. Hsu discloses that an electrode (23) can be polysilicon. It would have been obvious to use the polysilicon of Hsu in the device of Shinohe in order to use an electrode material that is well known and widely available in the art, as well as economically feasible.

Response to Arguments

7. Applicant's arguments with respect to claims 16, and 20 – 32 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
June 24, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800